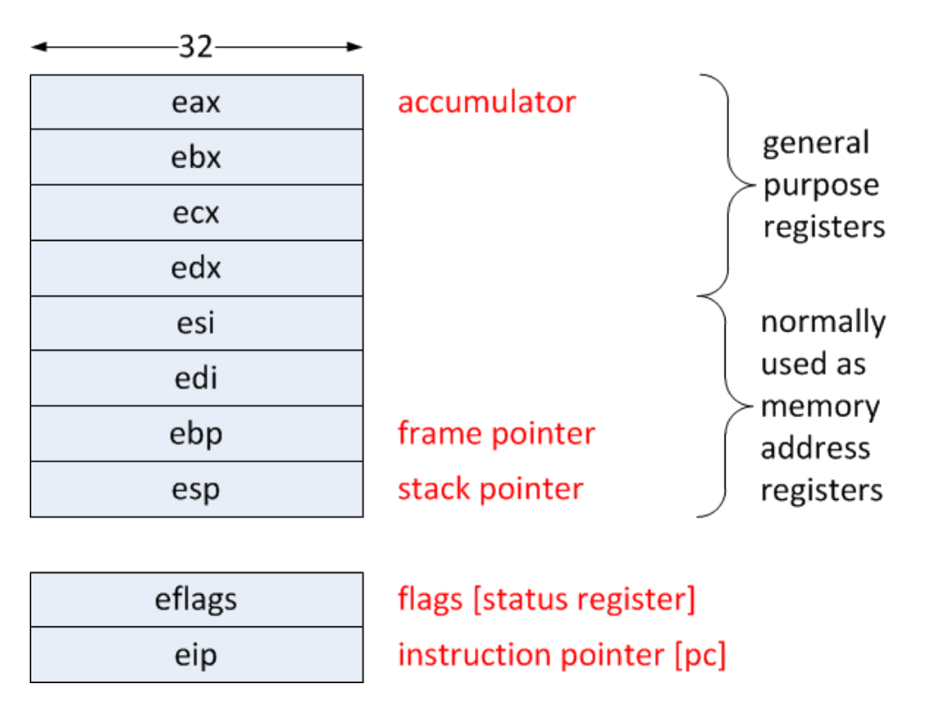
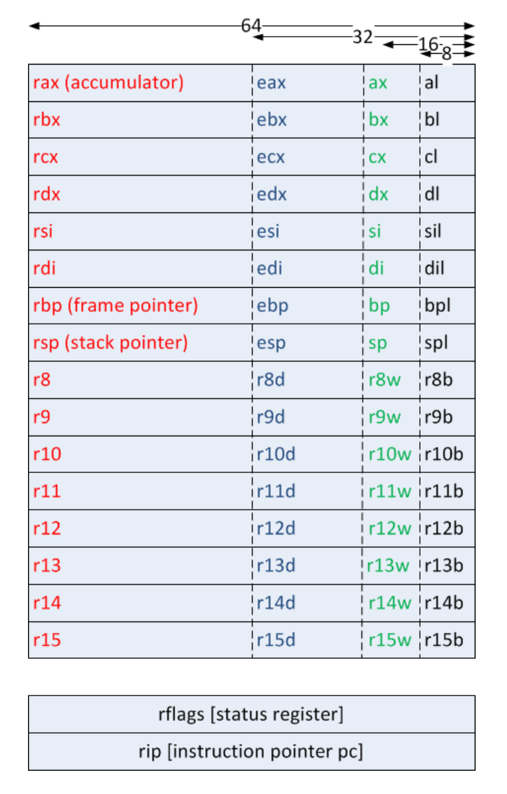
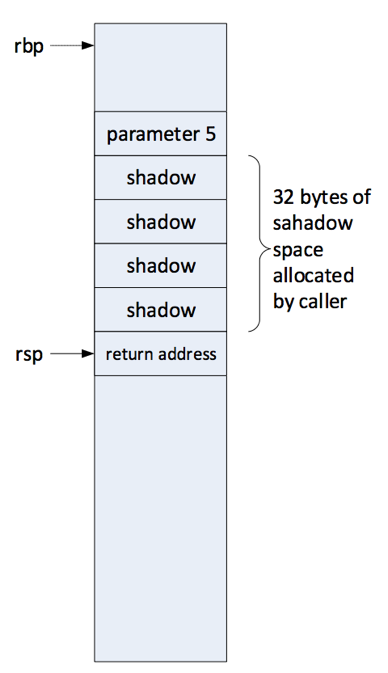
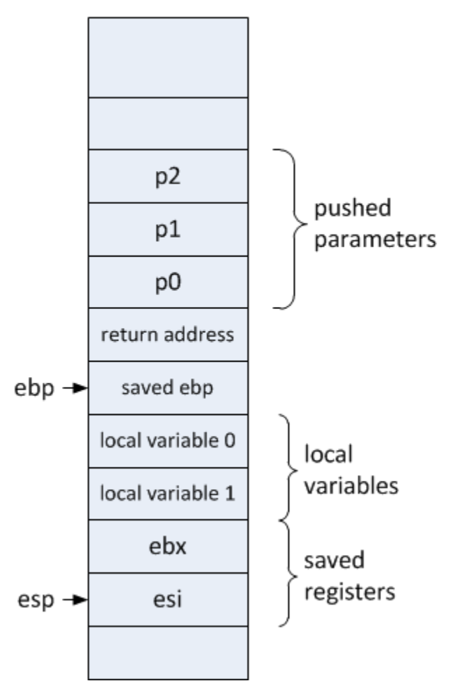
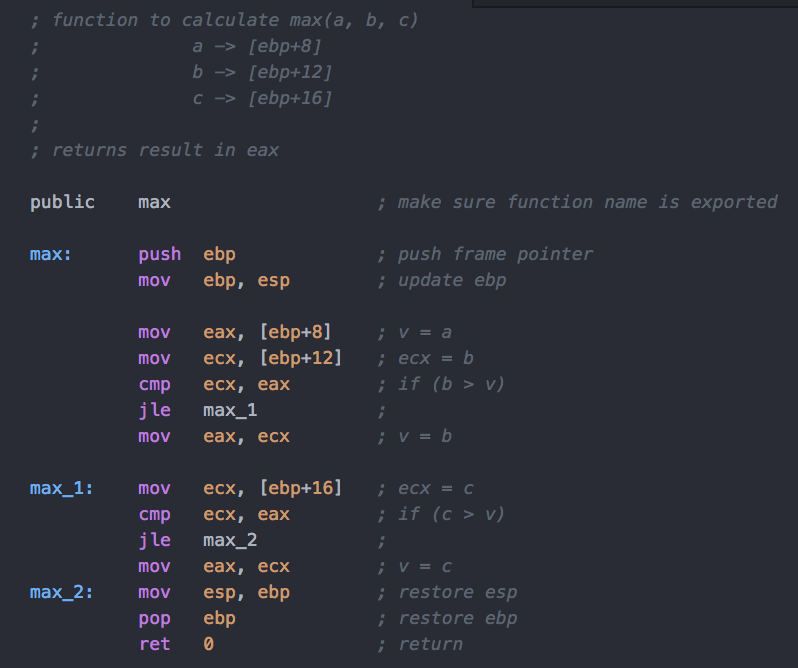
**Computer Architecture Exam Notes**

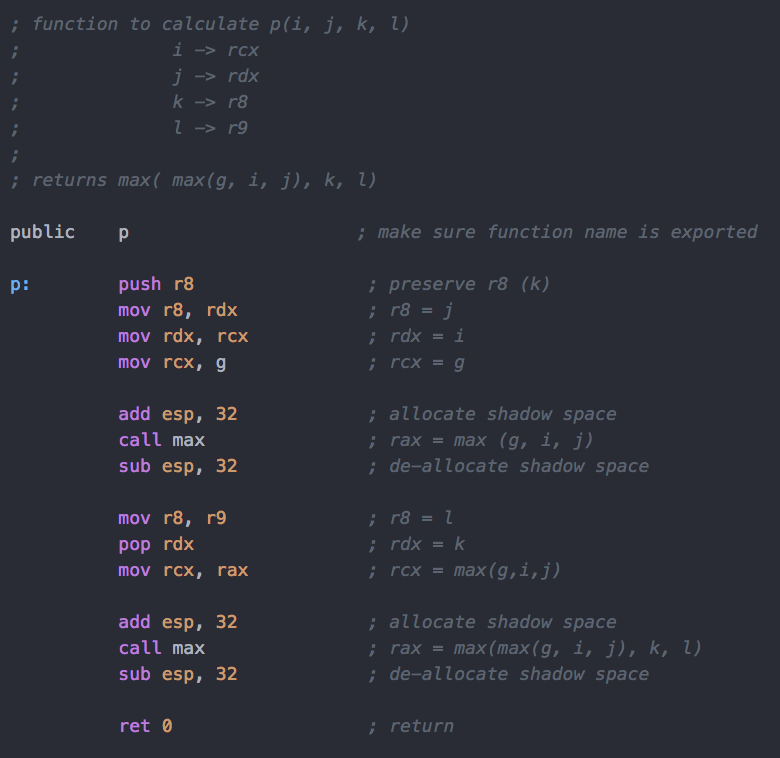
**Question 1 – 2018 (IA32 and x64)**

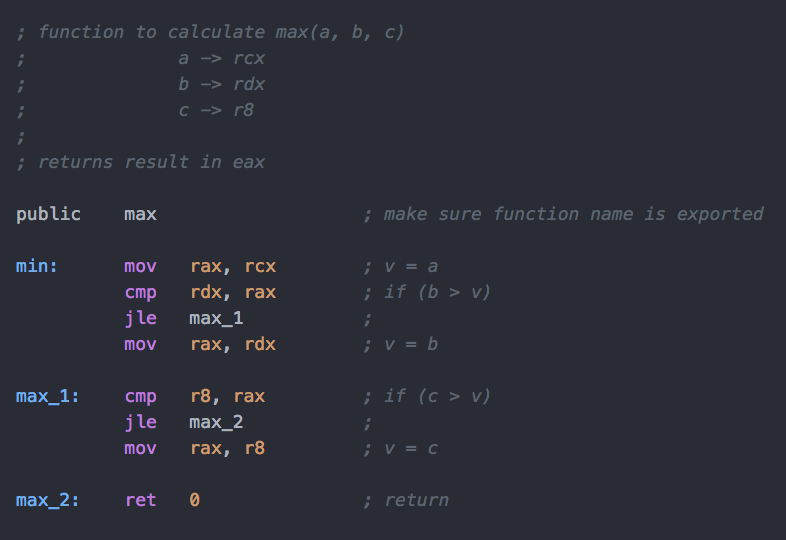
* CDECL used for C and C++
* Result always returned in eax and rax
* Parameters are pushed onto stack in reverse order
* Stack aligned on 4-bit and 8-bit boundary respectively
* X64 parameters pushed in rcx, rdx, r8, r9
* X64 uses 32-bytes of shadow space for parameters
* IA32 user must adjust stack
* In IA32 non-volatile registers are ebx
* In x64 non-volatile registers are rbx, r12-15



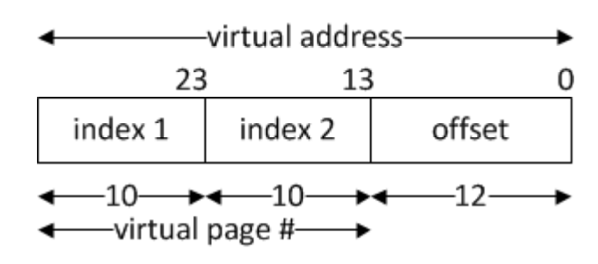


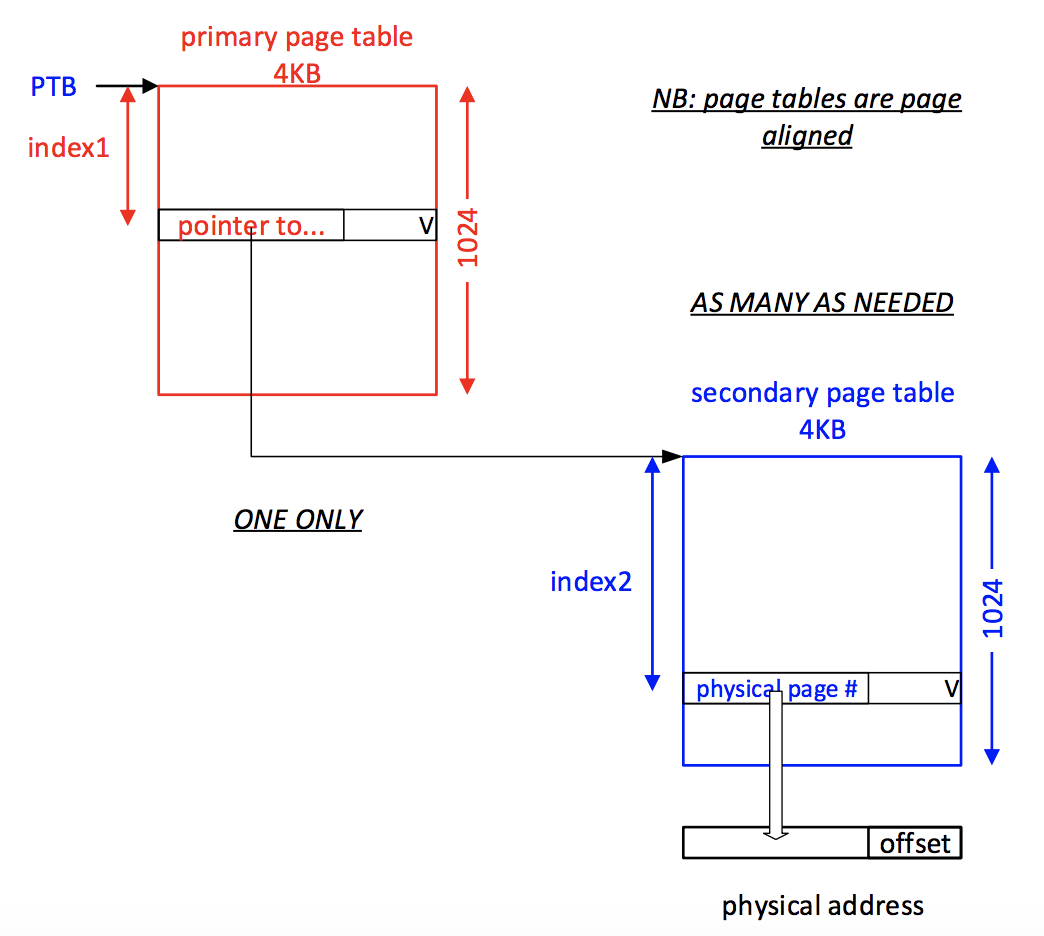






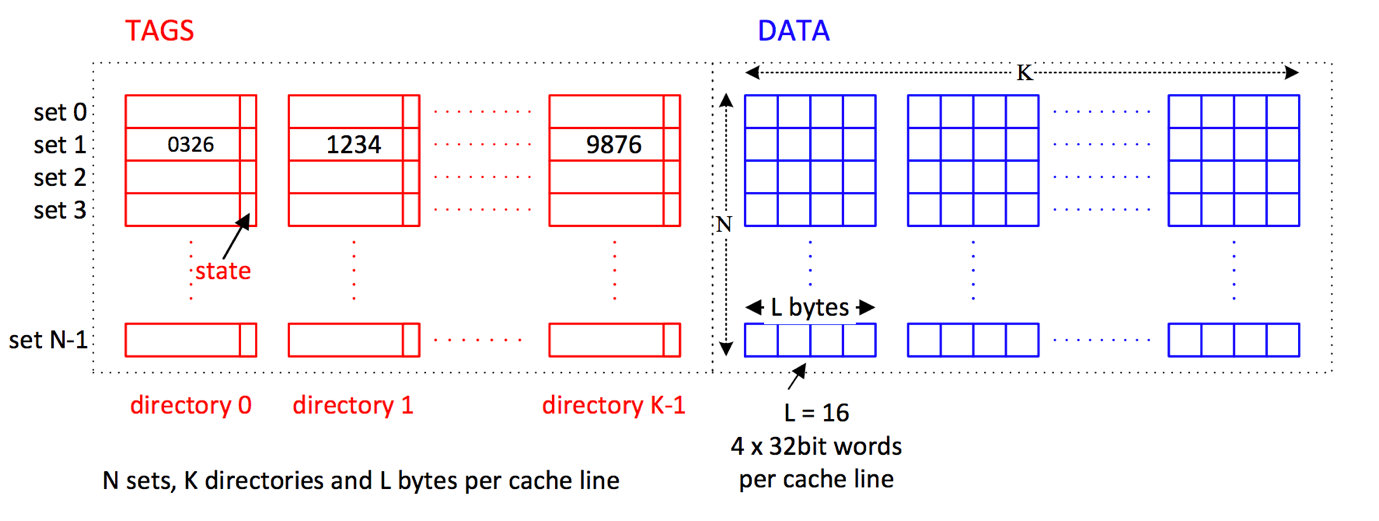
**Question 2 – 2018 (Page Tables)**

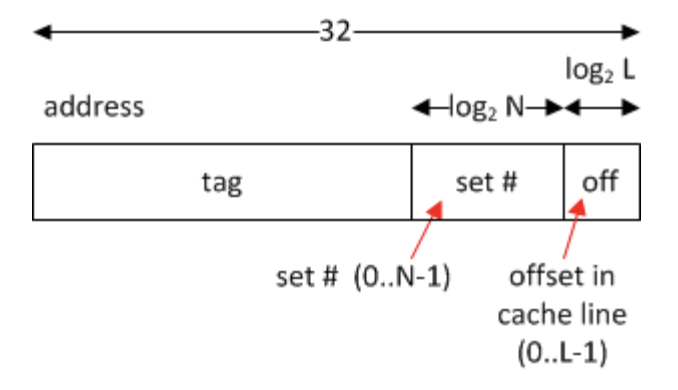




|  |  |  |
| --- | --- | --- |
|  | min process (i) | max process (ii) |
| 1 level page table | 4MB | 4MB |
| 2 level page table | 4KB + 4KB  (1 primary level table always present, smallest process will need at least one secondary) | 4KB + 4MB  (1 primary level table + 1024 secondary level tables) |

**Question 3 – 2018 (Cache)**

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* L = Bytes per cache line
* K = Directories across
* N = Sets down
* **Direct Mapped 🡪 K = 1**
* **Fully Associative 🡪 N = 1**

|  |  |
| --- | --- |
| 1. **64 byte Direct Mapped Cache**   - L = 16 bytes  - K = 1  - N = 4  - Offset: Last 4 bits  - Set: Next 2 bits  - Tag: Remaining bits | 1. **64 byte Fully Associative Cache**   - L = 16 bytes  - K = 4  - N = 1  - Offset: Last 4 bits  - Set: 0 BITS (only one set)  - Tag: Remaining bits |